One skilled in the art will appreciate that although the flowchart diagrams can be drawn in sequential order for comprehension, certain steps can be carried out in parallel in an actual implementation. Furthermore, unless indicate otherwise, method steps can me interchanged without departing form the scope of the invention.

Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

Those of skill would farther appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality can be implemented as hardware or software depends upon the particular application and design constraints imposed, on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may he embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium can be coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. For example, although the description specifies that the radio access network **20** can be implemented using the Universal Terrestrial Radio Access Network (UTRAN) air interface, alternatively, in a GSM/GPRS system, the access network **20** could be a GSM/EDGE Radio Access Network (GERAN), or in an inter-system case it could be comprise cells of a UTRAN air interface and cells of a GSM/EDGE air interface. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A method of receiving user information, comprising:

receiving an outer code block comprising a plurality of rows of information blocks, wherein the rows of information blocks each include at least a portion of a row of user information, wherein the size of each row of information blocks is fixed and occupies one Transmission Timing Interval (TTI);

decoding the outer code block using rows of redundancy information to generate a complete encoder packet that comprises information blocks and length indicators, wherein the information blocks are free from errors; and

using at least one length indicator in each information block to determine where a row of user information ends within the outer code block row occupied by that information block, and splitting the information blocks into rows of user information.

2. A method of receiving user information, comprising:

receiving an outer code block comprising a plurality of rows of information blocks, wherein the rows of information blocks: each include at least a portion of a row of user information, wherein the size of each row of information blocks is variable and the rows of user information fully occupy the plurality of rows of information blocks;

decoding the outer code block using rows of redundancy information to generate a complete encoder packet that comprises information blocks and length indicators, wherein the information blocks are free from errors; and

using at least one length indicator in each information block to determine where a row of user Information ends within the outer code block row occupied by that information block; and

splitting the information blocks into rows of user information.

3. A destination station, comprising:

a receive buffer that receives an outer code block comprising a plurality of rows of information blocks, wherein the rows of information blocks each include at least a portion of a row of user information, wherein the size of each row of information blocks is fixed and occupies one Transmission Timing Interval (TTI);

an outer decoder that decodes the outer code block using rows of redundancy information to generate a complete encoder packet that comprises information blocks and length indicators, wherein the information blocks free from errors; and

a reassembly unit that uses at least one length indicator in each information block to determine where a row of user